

2027 VLSI TSA

International VLSI Symposium on Technology, Systems and Applications

📅 April 12–16, 2027 📍 Hsinchu, Taiwan 



Call for Papers

Paper Submission Deadline: **23:59 (GMT+8) Sunday, November 22, 2026**
Details: <https://expo.itri.org.tw/2027VLSITSA>

HIGHLIGHTS

The 2027 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA 2027) will be held on April 12–16, 2027, at the Ambassador Hotel Hsinchu, Taiwan, with an optional excursion scheduled for April 16.

The 5-day main program will feature:

- 3 Plenary Sessions
- 2 Joint Special Sessions
- 2 Industrial Sessions
- 7 Special Sessions
- 3 Tutorials
- Outstanding Paper Presentations

GENERAL INSTRUCTIONS

- Prospective authors are invited to submit papers through the symposium website.
- Accepted papers **MUST** be presented in person by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore.
- Author Registration Policy:
 - One FULL Registration covers the publication of up to two accepted papers.
 - Each accepted paper must be covered by a valid full registration in order to be included in the symposium proceedings.
 - If a valid FULL Registration has not been received and processed for an accepted paper, the symposium organizers will contact the authors before the paper is removed from the proceedings.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.

TSA SCOPE: Submission to TSA <https://expo.itri.org.tw/2027VLSITSA/TSA/Submission>

■ ADVANCED LOGIC TECHNOLOGY

- Front-end Silicon CMOS and Foundry Platform Technology
- Advanced Process Modules and Nano-patterning, including EUV
- Advanced BEOL/Packaging and 2.5D/3D Heterogeneous Integration
- Advanced Manufacturing Technology, Metrology and Yield

■ NEUROMORPHIC, IN-MEMORY and NOVEL COMPUTING

- Neuromorphic Devices and Technologies for AI Hardware and In-Memory Computing
- Probabilistic, Stochastic and Optimization Computing
- Emerging Computing Architecture and Hardware Primitives

■ POWER, MILLIMETER WAVE AND ANALOG TECHNOLOGY

- Power Devices and Technologies Including Silicon and Wide Band Gap
- Analog/RF IC Device Technologies

■ RELIABILITY OF SYSTEMS and DEVICES

- Reliability Physics, Characterization and Test

■ EMERGING DEVICE and COMPUTE TECHNOLOGY

- Quantum Phenomena and Information Technologies
- Beyond Silicon Technologies including Low Dimensional Materials and Oxide Semiconductors

■ MODELING AND SIMULATION

- Modeling and Simulation, including DTCO

■ OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS

- Silicon Photonics and Integrated Optoelectronic Devices

■ MEMORY TECHNOLOGY

- Advanced Memory: DRAM, FLASH, Emerging Memories such as Resistive, Spintronic and Ferroelectric Devices

■ SENSORS, MEMS, and BIOELECTRONICS

- MEMS, Imagers and Sensors
- Flexible and Organic Electronics

DAT SCOPE: Submission to DAT <https://expo.itri.org.tw/2027VLSITSA/DAT/Submission>

■ Analog, Mixed-Signal, and RF Design

- Analog and Mixed-Signal Circuits
- Data Converters
- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wire Line System and IO Design
- Sensor and Interface Circuits

■ Digital, Memory, and AI Chip Design

- Asynchronous and Neuromorphic Computing Circuits
- Computing-in-Memory
- Digital AI Chips
- Digital Circuits and ASICs
- Hardware Optimizations for Novel Computation Models
- Hardware Security and Trust Circuits for IoT and AI
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems Including Reliability, Memory Architectures, and Emerging Memories

■ Application, Software and Hardware, and AI System

- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip)
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration

■ Design Automation and Test Methodology

- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

■ Emerging Technology

- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- ICs for Harsh Environments and Soft-Error
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

Symposium General Chair

Shih-Chieh Chang
Industrial Technology Research Institute

TSA Symposium Chair

Shimeng Yu
Georgia Institute of Technology

TSA Program Chairs

Ionut Radu
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Wei-Chung Lo
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National Taiwan University

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